Junbin **Lee**

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Profile

EDA software engineer with hands-on experience developing and improving design automation software for netlist optimization, Python/C++ hybrid development, and transistor-level physical design automation. Worked on core EDA workflows spanning circuit topology refinement and validation, performance-sensitive engine development, and GPU-accelerated placement-matrix generation. Contributed to improving reliability across complex design flows through core logic development, validation enhancements, and tighter integration between Python and C++ components. Background in AI-based EDA parameter optimization and circuit-similarity-driven design exploration provides a strong foundation in both implementation and optimization methodology.

Education

Sejong University Mar. 2020 – Feb. 2026
B.S. in Department of Electrical and Information Engineering
Total GPA of 4.25/4.5, Major GPA of 4.44/4.5 **Summa Cum Laude**

Experience

Axion CO., Ltd. **Pangyo, Republic of Korea**
EDA Engineer Jun. 2025 – Present

Work
- Researched and developed optimization algorithms for 4nm standard cell layout automation, including netlist optimization, topology refinement, and validation logic.
- Developed core software components for 4nm design automation, including transistor-level placement, layout candidate evaluation, and constraint validation.
- Built and maintained Python/C++ hybrid EDA engine components for performance-sensitive layout automation workflows.
- Developed C++/CUDA components for GPU-accelerated transistor-level placement, including warp-level kernel design and CPU/GPU consistency validation.

Impact
- Reduced CPP of production-level 4nm standard cells through layout-aware netlist optimization.
- Improved automation reliability and placement correctness by implementing validation and constraint-checking logic.
- Accelerated transistor-level placement exploration and design iteration through GPU-based candidate evaluation.
- Achieved up to 800× runtime improvement through warp-level parallelization.

VLS*i*CAD Lab, Sejong University **Seoul, Republic of Korea**
Undergraduate Student Researcher Aug. 2024 – Dec. 2024

Work
- Researched Design Compiler parameter optimization using genetic algorithms for logic synthesis optimization.
- Compared optimization performance by varying selection and mutation strategies in genetic algorithms.
- Analyzed the impact of initial population selection methods on Design Compiler parameter optimization performance.

Impact
- Achieved 33% runtime reduction and 15% EDP improvement through genetic algorithm-based Design Compiler parameter optimization.

PLANTNER INC. **Seoul, Republic of Korea**
Jan. 2023 – Nov. 2023

Cofounder, H/W Engineer

Work
- Researched measurement methods for plant growth hormones and designed hardware device concepts.
- Proposed SDG-aligned development cooperation initiatives for Vietnam and formulated support plans with KOICA.

Impact
- Secured KRW 200M in funding through selection for the KOICA CTS Seed Program.
- Selected for the Startup Promising Team 300 Growth Track.

United Nation Peacekeeping — **Tyre, Lebanese Republic**
Signalman — Jul. 2021 – Jan. 2022

Work
- Deployed overseas for a 6-month United Nations peacekeeping mission.
- Operated and maintained wireless communication systems

Publications

Conference

[1] **Junbin Lee**, Jinil An and Daijoon Hyun, "Circuit-Similarity-Based Parameter Optimization for Logic Synthesis Tools", Korean Conference on Semiconductors (KCS), 2025 **Best Paper Awarded**

Awards & Honors

Awards

2025.02	Best Paper Awarded – VLSI CAD	*KCS*
2025.01	Encouragement Award, AI Semiconductor Idea/Design Contest	*IITP*
2024.11	1st place, IT Creative Challenge	*IEIE*
2023.11	Encouragement Award, Industry-University Collaboration Expo	*KOEF*
2023.08	Certification, Selected for 2023 Promising Student Start-up Team 300	*Ministry of Education*
2023.08	1st place, Summer Start-up Bootcamp	*Sejong Univ.*
2023.05	2nd place, Start-up Idea Competition	*Sejong Univ.*

Honors

2024.01	2 Years Full-funded Scholarship	*KOSFFL*
2024.03	1st place, Academic Scholarship	*Sejong Univ.*
2023.09	3rd place, Academic Scholarship	*Sejong Univ*.

Research Skills

Linux

Programming
- Python, C++, CUDA

EDA Tools
SYNOPSYS
- Design Compiler, IC Compiler II, Primetime, Custom Compiler, Verdi

Cadence
- PSpice, OrCAD

KiCad
- Symbol Editor, Schematic Editor, Footprint Editor, PCB Editor

Intel
- Quartus Prime